



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

[Handwritten signature]

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,773	04/03/2000	Bryan Keith Bullis	RAL9-99-0137	4749

25299 7590 01/07/2004

IBM CORPORATION
PO BOX 12195
DEPT 9CCA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER

LEE, TIMOTHY L

ART UNIT PAPER NUMBER

2662

DATE MAILED: 01/07/2004

7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/541,773

Applicant(s)

BULLIS ET AL.

Examiner

Timothy Lee

Art Unit

2662

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 2-11 and 17-19 are objected to because of the following informalities: “a predetermined threshold” is mentioned in reference to the write process and the transfer process, but it is not entirely clear if this is there is one predetermined threshold or two different predetermined thresholds. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Egbert et al. (US 6,115,387).

4. Regarding claims 1, 11, and 12, Egbert et al. discloses a method for initiating and forwarding data from a device as a function of the data received at the device. Fig. 4 shows a block diagram of the output queue 74. See col. 8, lines 15-17. In operation, the output queue write side 76 receives an entry. After the entry flows through and reaches the bottom of the output queue write side 76, control logic associated with the output queue 74 makes a decision as to what to do with the entry. If there is space in the output queue read side 78, then one or more entries are passed directly from the output queue write side 76 to the output queue read side. See col. 8, lines 51-65. However, if the output queue read side 78 is full, then the output queue write

Art Unit: 2662

side will wait until after the output queue read side empties and has enough space to accommodate a burst-size amount of data—in other words, the output queue write side 76 will wait until the amount of empty space in the output queue read side 78 reaches a certain threshold before transferring data again (writing another data cell into the entry section...based on a predetermined threshold). Because the transfer is based on a certain amount of free space in the buffer, it is possible that the previous data cell is not finished emptying before this next transfer begins (prior the data cell being completely read in the entry section). It is also inherent that there must be a signal sent to the output queue write side 76 to inform it to commence the transfer of data to the read side (signaling circuit providing a write signal to the entry section to begin writing). See at least col. 9, lines 1-15. After the data is moved to the output queue read side 78, the transmission of data is controlled by the buffer manager 72, which begins moving frame data from the address specified by the frame pointer, and once the transmit FIFO of the MAC port has been primed to its start point, frame transmission commences—thus, the buffer manager 72 when data should be transmitted from one section to another (a signaling circuit coupled to the entry section for providing a signal to transfer a portion of data). In the first mode of the switch operation designed to provide the lowest latency, frames are received and forwarded at line-rate speed. In this mode, frame reception may not complete before frame transmission at the output ports commences (transfer a portion of a data cell prior to the data cell being completely received by the entry section). See col. 20, line 56-col. 21, line 36.

5. Regarding claim 2, Egbert et al. discloses that the port vector FIFO that there can be different thresholds, including receiving n bytes where $n < 64$ bytes (signal is provided once the

Art Unit: 2662

amount of data received by the entry section reaches a predetermined threshold). See col. 22, lines 1-11.

6. Regarding claim 3, the output queues 74 could be considered entry sections along with being buffer entry sections.

7. Regarding claim 4, Egbert et al. discloses that the system was designed as a switch for a packet switched network. As an example, ATM is a packet switched system. ATM is asynchronous (wherein signaling circuit comprises an asynchronous signaling circuit).

8. Regarding claim 13, the buffer manager controls all transmission of data across the switch, so by issuing a command for the output queue to receive data from the external memory, the output queue could begin receiving a new data cell before it is finished output the previous cell depending on when that command is issued.

9. Regarding claim 14, the output queues contain a read side and a write side as shown in Fig. 3 (buffer entry section comprises a write element and a read element). Egbert et al. also discloses that the system was designed as a switch for a packet switched network. As an example, ATM is a packet switched system. ATM is asynchronous (wherein signaling circuit comprises an asynchronous signaling circuit).

10. Regarding claim 15, the buffer controller controls all of the movement of data through the switch, so it is responsible for telling the output queues when to forward their data and for telling when the output queue should receive its data from the external memory (add signaling portion and a remove signaling portion).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 5-9 and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egbert et al. in light of the rejections above.

13. Regarding claims 5, 7, 8, and 16, Egbert et al. discloses that the output queues contain a read side and a write side as shown in Fig. 3 (buffer entry section comprises a write element and a read element). Queuing takes the form of the port vector FIFO 70 writing frame pointers into the various output queues 74 indicated in a forwarding port vector—these pointers must be responsible for keeping track where in the data it is being transmitted (entry pointer...an item pointer). See col. 10, lines 1-11. Egbert et al. does not expressly disclose having an entry counter within the buffer entry section, but Egbert et al. does disclose having an MIB counter region that keep tracks of statistics of all the ports. See col. 11, lines 36-42. It would have been obvious to put this counter functionality into the output queues section. One would have been motivated to do this because having the counters on the chip would allow for faster access to the values contained in the counters.

14. Regarding claims 6, 9, and 10, the buffer controller controls all of the movement of data through the switch, so it is responsible for telling the output queues when to forward their data and for telling when the output queue should receive its data from the external memory (add

Art Unit: 2662

signaling portion and a remove signaling portion). Also, the buffer controller can tell the output queue to access more data from the external memory by issuing a new port vector.

15. Regarding claim 17, it is inherent in Egbert et al. that the writing element would write the data cell into the output queue. Also, during operation, the output queue structure is acting most like a traditional queue, because it is from the portion that entries are taken, one by one. In a traditional queue, the pointer will naturally increment in order to output the next piece of data. Step a3 has been mentioned previously.

16. Regarding claim 18, it is inherent in Egbert et al. that if the pointer is being incremented, then there must be some sort of add signal.

17. Regarding claims 19 and 20, Egbert et al. does not expressly disclose incrementing a second entry counter. However, it would have been obvious to a person of ordinary skill in the art at the time of the invention to increment the second entry counter along with the first counter if another piece of data was to be transferred. One of ordinary skill in the art would have been motivated to do this because incrementing a separate counter could act as a confirmation for what the first counter value should be in case of an error in the system.

18. Regarding claim 21, it would be inherent to decrement the first counter if data is being extracted.

19. Regarding claim 22, the buffer controller controls all of the movement of data through the switch, so it is responsible for telling the output queues when to forward their data and for telling when the output queue should receive its data from the external memory (add signal and remove signal).

Art Unit: 2662

Response to Arguments

20. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection. The Examiner mistakenly allowed and/or objected to claims that should have been rejected in the previous Office Action based on a further reading of the reference.

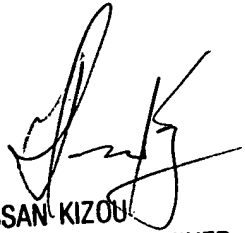
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy Lee whose telephone number is (703)305-7349. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703)305-4744. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

TLL


HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600